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VLSI Test Symposium, 1995. Proceedings., 13th IEEE , 30 April-3 May 1995
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2 **An integrated 16-channel CMOS time to digital converter**
Ljuslin, C.; Christiansen, J.; Marchioro, A.; Klingsheim, O.;
Nuclear Science, IEEE Transactions on , Volume: 41 Issue: 4 , Aug 1994
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3 **A vertically integrated test methodology based on JTAG IEEE 1149.1 Standard Interface**
Ruparel, K.N.; Chin, C.; Fitzgerald, J.;
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International , 23-27 Sept. 1991
Page(s): P11 -4/1-4

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4 **Functional test and diagnosis: a proposed JTAG sample mode scan tester**
Lefebvre, M.E.;
Test Conference, 1990. Proceedings., International , 10-14 Sept. 1990
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5 **Tradeoff decisions made for a P1149.1 controller design [ATE]**
Vining, S.;
Test Conference, 1989. Proceedings. 'Meeting the Tests of Time'., International , 29-31 Aug. 1989
Page(s): 47 -54

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6 **BIST and boundary-scan for board level test: test program pseudocode**
Tulloss, R.E.; Yau, C.W.;
European Test Conference, 1989., Proceedings of the 1st , 12-14 April 1989
Page(s): 106 -111

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---

7 **IEEE-1149.1 use in design for verification and testability at Texas Instruments**
Cron, A.D.;
ASIC Seminar and Exhibit, 1989. Proceedings., Second Annual IEEE , 25-28 Sept. 1989
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Page(s): 580 -585

[Abstract] [PDF Full-Text (548 KB)] **IEEE CNF**

2 **A method for synchronizing IEEE 1149.1 test access port for chip level testability access**
Bhavsar, D.;
VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on , 4-7 Jan. 1998
Page(s): 289 -292

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3 **System level boundary scan in a highly integrated switch**
Hughes, W.J.;
Test Conference, 1997. Proceedings., International , 1-6 Nov. 1997
Page(s): 636 -639

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4 **Experience of designing JTAG ASICS within System X**
Borland, A.;
Application and Development of the Boundary-Scan Standard, IEE Colloquium on , 19 Dec 1990
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Solid-State Circuits Conference, 1996. Digest of Technical Papers. 43rd ISSCC., 1996 IEEE International , 8-10 Feb. 1996
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Gallia, J.; Yee, A.; Wang, I.; Chau, K.; Davis, H.; Swamy, S.; Sridhar, T.; Nguyen, V.; Ruparel, K.; Moore, K.; Lemonds, C.; Chae, B.; Eyres, P.; Yoshino, T.; Pozadzides, J.; Rine, R.; Shah, A.;
Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989 , 15-18 May 1989
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Fall VIUF Workshop, 1999. , 4-6 Oct. 1999
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Yeandel, J.; Thulborn, D.; Jones, S.;
Circuits, Devices and Systems, IEE Proceedings- , Volume: 145 Issue: 1 , Feb. 1998
Page(s): 1 -6

[Abstract] [PDF Full-Text (632 KB)] **IEE JNL**

3 **An on-line testable UART implemented using IFIS**
Yeandel, J.; Thulborn, D.; Jones, S.;
VLSI Test Symposium, 1997., 15th IEEE , 27 April-1 May 1997
Page(s): 344 -349

[Abstract] [PDF Full-Text (524 KB)] **IEEE CNF**

4 **A 4*2.5 Mchip/s direct sequence spread spectrum receiver with digital IF and integrated ARM6 core**
Gyselinckx, B.; Rynders, L.; Engels, M.; Bolsens, I.;
Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997 , 5-8 May 1997
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[Abstract] [PDF Full-Text (424 KB)] **IEEE CNF**

5 **ARM7100-a high-integration, low-power microcontroller for PDA applications**
Budd, G.; Milne, G.;
Compcon '96. 'Technologies for the Information Superhighway' Digest of Papers , 25-28 Feb. 1996
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[Abstract] [PDF Full-Text (508 KB)] **IEEE CNF**

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Bush, D.;
WESCON/'95. Conference record. 'Microelectronics Communications Technology Producing Quality Products Mobile and Portable Power Emerging Technologies' , 7-9 Nov. 1995
Page(s): 377

[Abstract] [PDF Full-Text (384 KB)] **IEEE CNF**

---

7 **Rapid migration to VLSI**
Lowinski, W.B.; Kirwan, R.; Perry, A.; Yu, T.;
Aerospace and Electronics Conference, 1992. NAECON 1992., Proceedings of the IEEE 1992 National , 18-22 May 1992
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Lowinski, W.B.; Kirwan, R.; Perry, A.; Yu, T.;
Aerospace and Electronic Systems Magazine, IEEE , Volume: 7 Issue: 9 , Sept. 1992
Page(s): 21 -23

[Abstract] [PDF Full-Text (216 KB)] **IEEE JNL**

---

9 **Sendfax a single chip fax and data modem**
Lindsay, G.;
Circuits and Devices for Data Communications, IEE Colloquium on , 28 Nov 1989
Page(s): 3/1 -3/5

[Abstract] [PDF Full-Text (200 KB)] **IEE CNF**

---

10 **A single-chip 300 baud FSK modem**
Takla, A.K.; Haque, V.A.;
Solid-State Circuits, IEEE Journal of , Volume: 19 Issue: 6 , Dec 1984
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[Abstract] [PDF Full-Text (920 KB)] **IEEE JNL**

---

11 **MTEC: A Microprocessor System for Astronomical Telescope and Instrument Control**
Ellis, M.J.; Hovey, G.R.; Stapinski, T.E.;
Solid-State Circuits, IEEE Journal of , Volume: 15 Issue: 1 , Feb 1980
Page(s): 144 -147

[Abstract] [PDF Full-Text (584 KB)] **IEEE JNL**

---

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Tierney, J.; Walrod, R.;
OCEANS , Volume: 9 , Sep 1977
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Document Analysis and Recognition, 1999. ICDAR '99. Proceedings of the Fifth International Conference on , 20-22 Sept. 1999
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Data Compression Conference, 1999. Proceedings. DCC '99 , 29-31 March 1999
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3 **Information technology - telecommunications and information exchange between systems - local and metropolitan area networks - specific requirements. Part 5: token ring access method and physical layer specifications**
ISO/IEC 8802-5, ANSI/IEEE Std 802.5, 3rd edn. 1998 , 26 May 1998

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4 **Feature-based Thai unknown word boundary identification using Winnow**
Charoenpornsawat, P.; Kijsirikul, B.; Meknavin, S.;
Circuits and Systems, 1998. IEEE APCCAS 1998. The 1998 IEEE Asia-Pacific Conference on , 24-27 Nov. 1998
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[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

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Rufino, J.; Verissimo, P.; Arroz, G.; Almeida, C.; Rodrigues, L.;
Fault-Tolerant Computing, 1998. Digest of Papers. Twenty-Eighth Annual International Symposium on , 23-25 June 1998
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[Abstract] [PDF Full-Text (272 KB)] **IEEE CNF**

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Shi, Z.; Srihari, S.N.; Shiu, Y.-C.; Ramanaprasad, V.;
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ISO/IEC Std 8802-5, 1995, ANSI/IEEE Std 802.5-1995 , 29 Dec. 1995

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8 **4.0 Structure Delimiter Statements**
IEEE Std 716-1995 , 12 Oct. 1995
Page(s): 9

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9 **A language for document generic layout description and its use for segmentation into regions**
Azokly, A.; Ingold, R.;
Document Analysis and Recognition, 1995., Proceedings of the Third International Conference on , Volume: 2 , 14-16 Aug. 1995
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Yoshida, Y.; Mizoe, K.; Matsuda, A.; Kuroiwa, S.;
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---

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Visual Languages, 1992. Proceedings., 1992 IEEE Workshop on , 15-18 Sept. 1992
Page(s): 264 -266

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---

12 **Text compression using several Huffman trees**
Basu, D.;
Data Compression Conference, 1991. DCC '91. , 8-11 April 1991
Page(s): 452

[Abstract] [PDF Full-Text (52 KB)] **IEEE CNF**

---

13 **Frame content independent stripping for token rings**

Ramakrishnan, K.K.; Yang, H.;
Local Computer Networks, 1990. Proceedings., 15th Conference on , 30 Sept.-3 Oct. 1990
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14 **Description of and experimental results for a high data rate underwater acoustic telemetry link**
Estes, L.E.; Fain, G.; Caron, P.;
Autonomous Underwater Vehicle Technology, 1990. AUV '90., Proceedings of the (1990) Symposium on , 5-6 June 1990
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[Abstract] [PDF Full-Text (356 KB)] **IEEE CNF**

---

15 **Error characteristics of fiber distributed data interface (FDDI)**
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Communications, IEEE Transactions on , Volume: 38 Issue: 8 , Aug. 1990
Page(s): 1244 -1252

[Abstract] [PDF Full-Text (944 KB)] **IEEE JNL**

---

16 **Access control module for local integrated optical network**
Pallios, V.; Antonakopoulos, T.; Makios, V.;
Electronics Letters , Volume: 25 Issue: 3 , 2 Feb. 1989
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17 **A high speed access mechanism for a multiservice LAN at 144 Mbps**
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Electrotechnics, 1988. Conference Proceedings on Area Communication, EUROCON 88., 8th European Conference on , 13-17 June 1988
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18 **On the Impact of HDLC Zero Insertion and Deletion on Link Utilization and Reliability**
Joong Ma;
Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 30 Issue: 2 , Feb 1982
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19 **The parsing program for automatic text-to-speech synthesis developed at the electrotechnical laboratory in 1968**
Umeda, N.; Teranishi, R.;
Acoustics, Speech, and Signal Processing [see also IEEE Transactions on Signal Processing], IEEE Transactions on , Volume: 23 Issue: 2 , Apr 1975
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Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997
In this paper, we propose a method to generate high quality test waveform on chip to avoid the parasitic effects in an analog testability bus test environment. For the test response analysis, we derive an extraction methodology to remove the parasitic effects and obtain the intrinsic response of the CUT. The test results show that the algorithm is robust such that the intrinsic responses remain the same regardless of the small variation in the test waveforms. With the concept of intrinsic respon ...

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This paper proposes a new methodology for testing a core-based system-on-chip (SOC), targeting the simultaneous reduction of test area overhead and test application time. Testing of embedded cores is achieved using the transparency properties of surrounding cores. At the core level, testability and transparency can be achieved by reusing existing logic inside the core, and providing different versions of the core having different area overheads and transparency latencies. At the chi ...

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Kwang-Ting Cheng
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